REMARKS/ARGUMENTS

The amendments described in the following sections are made with the intention of placing the application in condition for allowance.

1. Objection to the drawings:

Fig.3, which illustrates a prior art, has been designated by a legend "Prior Art" as shown in the encircled area of the attached "Annotated sheet". No new matter is introduced by the above amendments. Consideration of the proposed amendment to the drawings is politely requested.

2. Rejection of claims 1-9 under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. in view of Fan et al.:

Claim 1 of the present application recites a flash memory cell structure comprising:

a substrate having a stacked gate;

a select gate formed on the substrate and adjacent to one side of the stacked gate;

a first-type doped region located in the substrate and adjacent to the select gate as a drain;

a shallow second-type doped region located underneath the stacked gate and adjacent to the first-type doped region;

a deep second-type doped region surrounding the first-type doped region and adjacent to the shallow second-type doped region; and

a doped source region formed on a side of the shallow second-type doped region as a source.

With regard to a cited prior art, Hsu discloses a flash memory cell structure 200 comprising:

a substrate 20 having a stacked gate G;

a first-type ion doped region 25 disposed in the substrate 20;

a shallow second-type ion doped region 26;

a deep second-type ion doped region 27 beneath the first-type ion doped region 25; and

a doped region 28 formed adjacent the shallow second-type ion doped region 26 as a source.

With regard to the other cited prior art, Fan discloses a flash memory cell comprising a select gate 18 formed on a substrate and adjacent to one side of the stacked gate.

As described, Hsu discloses a flash memory cell structure 200 comprising all the elements of the present application, except for the select gate. Fan also discloses a flash memory cell in which the select gate is formed on the substrate and adjacent to the stacked gate. The examiner asserts that it would have been obvious to one of ordinary skill in the art to incorporate Fan's teaching into and modify Hsu's teaching to arrive claim 1 of the present application.

The applicant, however, disagrees and asserts that it would not have been obvious to one of ordinary skill in the art to incorporate Fan's teaching into Hsu's teaching to achieve the claimed invention for the following reasons. First, Hsu does not teach or suggest any use of the select gate. In addition, although Fan discloses a flash memory cell having

a select gate, Fan does not teach or suggest that the select gate could be adopted to the flash memory cell structure as Hsu disclosed. Accordingly, the program, erase, and read mechanism of the flash memory cell structure taught by Hsu and Fan are different from the flash memory cell structure of the claimed invention. In addition, the flash memory cell structure of the claimed invention is able to inhibit the edge program disturb and the over program problem which Hsu and Fan do not mention in their teachings. Thus, the flash memory cell structure recited in claim 1 of the present invention is able to achieve unexpected results that Hsu and Fan perceived. Therefore, the applicant believes that claim 1 of the present invention is not obvious to one of ordinary skill in the art. Thus, reconsideration of claim 1 is respectfully requested.

3. Rejection of claims 2-9 under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. in view of Fan et al.:

Claims 2-9 are dependent on claim 1 and should be allowed if claim 1 is allowed. Reconsideration of claims 2-9 in view of the arguments made in section 2 above is therefore respectfully requested.

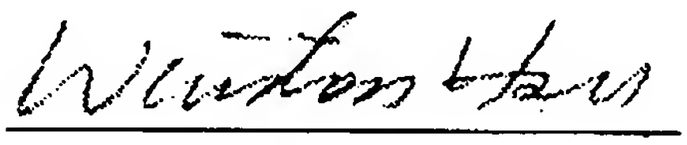
4. New claims 17-25:

Claim 17 recites a flash memory cell structure in which the limitation "the select gate being able to prevent an edge program disturb issue and an over program problem" is included. Specifically, the flash memory cell structure claimed in claim 17 is able to prevent the edge program disturb issue and the over program problem that the conventional flash memory cell structure suffers from. This limitation finds supports in the

specification, such as in paragraph [0010], and no new matter is entered. Thus, claim 17 of the present application includes a novel and unobvious limitation. Consideration of new claim 17 is respectfully requested. Claims 18-25 are dependent on claim 17, and should be allowed if claim 17 is allowed. Consideration of claims 18-25 is therefore politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



Date: May 12, 2005

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan).

Attachment:

The attachment (2 pages) includes a "Replacement Sheet" of Fig.3 and an "Annotated Sheet" showing changes.